**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1-5. (canceled).

6. (currently amended) A circuit, comprising:

a trigger control that adjusts rise and fall time settings of a clock;

a first register coupled to the trigger control, the first register to contain [[a]] default rise and fall settings of the clock, the trigger control ~~uses~~ using the rise and fall settings to adjust the clock;

m registers coupled to the first register with "m" being an integer greater than or equal to one, each of the m registers ~~has~~ having rise and fall settings that increase a period of the clock, the trigger control ~~accesses~~ accessing the m registers if a power supply voltage is detected to be less than a reference voltage; and

n registers coupled to the m registers with "n" being an integer greater than ~~two~~ or equal to one, the n registers having rise and fall settings that allow the clock to recover ~~the~~ a period ~~increases~~ increase from the m registers and a total decrease in clock period caused by the rise and fall settings of the n registers is less than a frequency guard band.

7. (currently amended) The circuit of claim 6, wherein the ~~n registers have~~ rise and fall settings ~~that allow the clock to recover the period increases from~~ stored in the m and n registers corresponding to stretching and reducing the clock period during first and second phases, respectively.

8. (canceled).

9. (original) The circuit of claim 7, wherein the m registers and the n registers are preset via fuses.

10. (original) The circuit of claim 7, wherein the m registers and the n registers are preset via metal options.

11. (original) The circuit of claim 7, wherein the m registers and the n registers are revised via a TAP controller.

12. (original) The circuit of claim 7, wherein the m registers and the n registers are revised via a microprocessor status register.

13. (original) The circuit of claim 7, wherein the m registers and the n registers are revised via a processor abstract layer.

14. (currently amended) The circuit of claim 6, further comprising:

a clock edge control buffer coupled to the trigger control, the clock edge control buffer ~~uses~~ using the rise and fall settings provided by the trigger control to independently adjust ~~the~~ clock rise and fall edge timings.

15-17. (canceled).

18. (currently amended) A method, comprising:

detecting a droop in a power supply voltage applied to an integrated circuit;

generating a droop trigger;

accessing rise and fall delay ~~values~~ settings of a clock from a plurality of registers; and

adjusting ~~the~~ rise and fall ~~edge~~ delays of the clock based on the rise and fall delay settings so that a total reduction of a clock period ~~of the clock~~ does not exceed a frequency guard band of the integrated circuit.

19. (currently amended) The method of claim 18, further comprising:

programming the plurality of registers with rise and fall delay ~~values~~ settings.

20. (currently amended) The method of claim 18, wherein adjusting the rise and fall ~~edge~~ delays of the clock comprises stretching the clock period.

21. (currently amended) The method of claim 20, wherein adjusting the rise and fall ~~edge~~ delays of the clock comprises recovering delays added to the clock during stretching of the clock period.

22-23. (canceled).

24. (currently amended) A circuit comprising:

a first register including [[a]] default rise and fall settings of a clock signal;

a first plurality of registers that include a rise and fall settings for increasing a clock period of the clock signal, the first plurality of registers being accessed if a power supply voltage is detected to be less than a reference voltage;

a second plurality of registers that include rise and fall settings for allowing the clock signal to recover ~~the increases~~ an increase of the clock period from the first plurality of registers ~~where~~ such that a total decrease in the clock period caused by the rise and fall settings of the second plurality of registers ~~being~~ is less than a frequency guard band; and

a trigger control in communication with the first register, the trigger control using the rise and fall ~~time~~ settings from the first register and accessing the rise and fall settings of the first plurality of registers if a power supply voltage is detected to be less than the reference voltage.

25. (previously presented) The circuit of claim 24, wherein the first plurality of registers and the second plurality of registers are preset via one of fuses or metal options.

26. (previously presented) The circuit of claim 24, wherein the first plurality of registers and the second plurality of registers are revised via a TAP controller.

27. (previously presented) The circuit of claim 24, wherein the first plurality of registers and the second plurality of registers are revised via a microprocessor status register.

28. (previously presented) The circuit of claim 24, wherein the first plurality of registers and the second plurality of registers are revised via a processor abstract layer.

29. (currently amended) The circuit of claim 24, further comprising:

a clock edge control buffer coupled to the trigger control, the clock edge control buffer to use the rise and fall settings provided by the trigger control to independently adjust ~~the~~ clock rise and fall edge timings.

30. (currently amended) A method, comprising:

detecting a droop in a power supply voltage applied to an integrated circuit;

accessing rise and fall delay ~~values~~ settings from a plurality of registers; and

adjusting ~~the~~ rise and fall ~~edge~~ delays of a clock signal based on the rise and fall delay settings so that a total reduction of a period of the clock signal does not exceed a frequency guard band of the integrated circuit.

31. (currently amended) The method of claim 30, further comprising:

programming the plurality of registers with rise and fall delay ~~values~~ settings prior to detecting the droop in the power supply voltage; and

generating a droop trigger signal in response to detecting the droop in the power supply voltage.

32. (currently amended) The method of claim 30, wherein adjusting the rise and fall ~~edge~~ delays of the clock comprises increasing the clock period.

33. (currently amended) The method of claim 30, wherein adjusting the rise and fall ~~edge~~ delays of the clock comprises recovering delays added to the clock signal during increasing of the clock period.

34. (currently amended) A circuit comprising:

a first register including a default rise and fall settings of a clock signal;

a plurality of registers including (1) rise settings to increase a clock period of the clock signal if a power supply voltage is detected to be less than a reference voltage and (2) fall settings to allow the clock signal to recover ~~the increases~~ an increase of the clock period from ~~the~~ a first plurality of registers where a total decrease in the clock period caused by the rise and fall settings of ~~the~~ a second plurality of registers ~~being~~ is less than a frequency guard band; and

a trigger control in communication with the first register and the plurality of registers to alter the clock period of the ~~clocking~~ clock signal.